AMENDMENTS TO THE CLAIMS

1. (Canceled).

2. (Currently Amended) The processor according to Claim 20~~1~~, further comprising a cache memory logically connected to the data bus in a second-endian byte order ~~based on the endianness of the processor~~,

wherein the processor reads data from the memory through the cache memory in data units of the same width as the data bus.

3. (Currently Amended) The processor according to Claim 20~~1~~, executing a program that defines structure data which includes data that is smaller than a basic word length, said structure data being shared between ~~the~~said processor and a first-endian type processor~~another processor of a different endianness~~ via the memory, said data being defined in an order within the basic word length, and said order being in reverse to an order in a definition of said structure data in a program to be executed by the first-endian type ~~said another~~ processor.

4. (Currently Amended) The processor according to Claim 3, further comprising a cache memory logically connected to the data bus in a second-endian byte order ~~based on the endianness of the processor~~,

wherein the processor reads data from the memory through the cache memory in data units of the same width as the data bus.

5. (Canceled).

6. (Currently Amended) The data sharing apparatus according to Claim 23~~5~~, further comprising an address conversion unit operable to convert at least one lower bit of an address so as to indicate a reversed position of data in the data bus, and output the converted address to the memory, when the second-endian processor performs a memory access for the data with a smaller width than the width of the data bus, and operable to

not convert any address when the processor performs a memory access for data having the width of the data bus.

7. (Currently Amended) The data sharing apparatus according to Claim 6, further comprising a transfer unit operable to control data transfer by direct memory access,

wherein, in the case where a source and a destination require data of different endianness and data with a smaller width than the width of the data bus is to be transferred, the transfer unit reverses an order of said data within a basic word length, for the source and the destination.

8. (Currently Amended) The data sharing apparatus according to Claim 7,

wherein the transfer unit includes a conversion unit operable to convert at least one lower bit of an address of either the source or the destination so as to indicate a reversed position of the data in the data bus, and output the converted address to the memory, in the case where a source and a destination require data of different endianness and data with a smaller width than the width of the data bus is to be transferred.

9. (Currently Amended) The data sharing apparatus according to Claim 6,

wherein the memory stores structure data to be accessed by ~~a~~the first-endian processor and ~~a~~the second-endian processor,

the first-endian processor executes a first program that defines the structure data, and

the second-endian processor executes a second program that defines structure data which includes data that is smaller than the basic word length, said data being defined in an order within the basic word length, and said order being in reverse to an order in the first program.

10. (Currently Amended) The data sharing apparatus according to Claim 9, further comprising a transfer unit operable to control data transfer by direct memory access,

wherein, in the case where a source and a destination require data of different endianness and data with a smaller width than the width of the data bus is to be

transferred, the transfer unit reverses an order of said data within a basic word length, for the source and the destination.

11. (Currently Amended) The data sharing apparatus according to Claim 10,

wherein the transfer unit includes a conversion unit operable to convert at least one lower bit of an address of either the source or the destination so as to indicate a reversed position of the data in the data bus, and output the converted address to the memory, in the case where a source and a destination require data of different endianness and data with a smaller width than the width of the data bus is to be transferred.

12. (Currently Amended) The data sharing apparatus according to Claim 23~~5~~, further comprising a cache memory logically connected to the data bus in a second-endian byte order ~~based on the endianness of the second processor~~.

13. (Currently Amended) The data sharing apparatus according to Claim 12, further comprising an address conversion unit operable to convert at least one lower bit of an address so as to indicate a reversed position of data in the data bus, and output the converted address to the memory, when the second processor performs a memory access for the data with a smaller width than the width of the data bus.

14. (Currently Amended) The data sharing apparatus according to Claim 13, further comprising a transfer unit operable to control data transfer by direct memory access,

wherein, in the case where a source and a destination require data of different endianness and data with a smaller width than the width of the data bus is to be transferred, the transfer unit reverses an order of said data within a basic word length, for the source and the destination.

15. (Currently Amended) The data sharing apparatus according to Claim 14,

wherein the transfer unit includes a conversion unit operable to convert at least one lower bit of an address of either the source or the destination so as to indicate a reversed position of the data in the data bus, and output the converted address to the

memory, in the case where a source and a destination require data of different endianness and data with a smaller width than the width of the data bus is to be transferred.

16. (Currently Amended) The data sharing apparatus according to Claim 13

wherein the memory stores structure data to be accessed by ~~a~~the first-endian processor and ~~a~~the second-endian processor,

the first-endian processor executes a first program that defines the structure data, and

the second-endian processor executes a second program that defines structure data which includes data that is smaller than the basic word length, said data being defined in an order within the basic word length, and said order being in reverse to an order in the first program.

17. (Currently Amended) The data sharing apparatus according to Claim 16, further comprising a transfer unit operable to control data transfer by direct memory access,

wherein, in the case where a source and a destination require data of different endianness and data with a smaller width than the width of the data bus is to be transferred, the transfer unit reverses an order of said data within a basic word length, for the source and the destination.

18. (Currently Amended) The data sharing apparatus according to Claim 17,

wherein the transfer unit includes a conversion unit operable to convert at least one lower bit of an address of either the source or the destination so as to indicate a reversed position of the data in the data bus, and output the converted address to the memory, in the case where a source and a destination require data of different endianness and data with a smaller width than the width of the data bus is to be transferred.

19. (Currently Amended) A method of sharing data in a data processing apparatus which includes a first-endian type processor and a second-endian type processor ~~of different endianness~~, and a memory to which both processors ~~the first processor and the second processor~~ are connected via a data bus~~,~~ in a first-endian byte order ~~based on the~~

~~endianness of the first processor~~, the method comprising:

~~a step of~~ causing the second processor to execute a program that defines structure data which includes data that is smaller than a basic word length, said structure data being shared in the memory, said data being defined in an order within the basic word length, and said order being in reverse to an order in a definition of said structure data for the first-endian type processor, and

~~a conversion step of converting~~ performing an address conversion on at least one lower bit of an address so as to indicate a reversed position of data in the data bus, in the case where the second-endian processor performs a memory access for data with a smaller width than the width of the data bus, and not performing the address conversion in the case where the second-endian processor performs a memory access for data having the width of the data bus.

20. (New) A processor connected to a memory via a data bus, the data bus having a data width, said processor being a second-endian type processor which is usable with a first-endian type processor, said processor comprising:

a processor bus logically connected to the data bus in a first-endian byte order; and

an address conversion unit operable to perform an address conversion on at least one lower bit of an address so as to indicate a reversed position of data in the data bus, and output the converted address to the memory, when the processor performs a memory access for data having a smaller width than the width of the data bus, and operable to not perform the address conversion when the processor performs a memory access for data having the width of the data bus.

21. (New) The processor according to claim 20, wherein the first-endian type is big-endian and the second-endian type is little-endian.

22. (New) The processor according to claim 20, wherein the first-endian type is little-endian and the second-endian type is big-endian.

23. (New) A data sharing apparatus comprising:

a data bus having a data width;

a memory;

a first-endian processor logically connected to said memory in a first-endian byte order via said data bus;

a second-endian processor logically connected to said memory in the first-endian byte order via said data bus; and

an address conversion unit operable to perform an address conversion on at least one lower bit of an address so as to indicate a reversed position of data in the data bus, and output the converted address to the memory, when the second-endian processor performs a memory access for data having a smaller width than the width of the data bus, and operable to not perform the address conversion when the processor performs a memory access for data having the width of the data bus.

24. (New) The data sharing apparatus according to claim 23, wherein the first-endian type is big-endian and the second-endian type is little-endian.

25. (New) The data sharing apparatus according to claim 23, wherein the first-endian type is little-endian and the second-endian type is big-endian.

26. (New) The method according to claim 19, wherein the first-endian type is big-endian and the second-endian type is little-endian.

27. (New) The method according to claim 19, wherein the first-endian type is little-endian and the second-endian type is big-endian.